ABSTRACT

A reconfigurable data processing apparatus. In this apparatus, many cells A 100 for performing ALU processing and cells B 150 for performing bit processing are arranged, each cell includes n-bit input/output ports and the cells are connected through a network with n-bit buses. Furthermore, when the number of output bits is smaller than n, cell B 150 fixes bits of orders irrelevant to outputs to "0" or "1." When the bussed ALU processing part and bit processing part are combined to perform data processing, this makes it possible to execute ALU processing and bit processing efficiently and realize high-speed, parallel processing.